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ART UNIT	PAPER NUMBER
2136	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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	Application No.	Applicant(s)	
Office Action Summary	10/786,966	CHO ET AL.	
	Examiner	Art Unit	
	OSCAR A. LOUIE	2136	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>15 January 2007</u>.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>5-8,13-16,18-21,24-27,32-34 and 43</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>5-8,13-16,18-21,24-27,32-34 and 43</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

This final action is in response to the amendment filed on 01/15/2007. In light of the applicant's amendments, the examiner hereby withdraws his previous Specification Objection and Claim 30 Objection. Claims 5-8, 13-16, 18-21, 24-27, 32-34, & 43 are pending and have been considered as follows.

Claim Objections

1.   Claim 13 is objected to because of the following informalities:

-    Claim 13 line 17 recites "The method of claim 9" which appears to be a typographical error and should be omitted;

   Appropriate correction is required.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

   A person shall be entitled to a patent unless –

   (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.   Claims 5, 8, 13, 16, 18-21, 24-27, 32, & 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Dalmia et al. (US-5835501-A).

Claim 5:

Dalmia et al. disclose a method of testing a serial transceiver chip for jitter tolerance, the

transceiver including at least one transmitter and at least one receiver comprising,

- "generating a serialization clock" (i.e. "The data generator 2 generates a data stream in a
  well known manner, the data timing of which is controlled by a clock signal received at
  the clock input of the data generator") [column 3 lines 17-19];

- "adding one or more known and controlled amount of jitter to the serialization clock" (i.e.
  "It is preferred that the data generator generates an arbitrary (pseudo random) data
  stream. In the present invention the timing of the clock is jittered by frequency or phase
  modulation") [column 4 lines 20-23];

- "transmitting a known sequence of test signals using the serialization clock with the
  added jitter" (i.e. "This provides a jitter of known characteristics of frequency or
  frequency and amplitude on the clock. The result is a jittered clock output, which is
  applied to the clock input of the data generator 2") [column 3 lines 27-31];

- "causing a clock and data recovery mechanism in a receiver to recover the test signals"
  (i.e. "The jitter test determines whether the CRU can correctly recover the data from the
  data stream that is generated from the specifically jittered clock") [column 3 lines 32-34];

- "comparing the recovered test signals with said known sequence of test signals thereby
  testing the ability of the clock and data recovery mechanism to tolerate the jitter that was
  added" (i.e. "The error detection circuit 3 checks the recovered data stream for bit errors,

the output thereof being an indication of the bits in error. Several realizations of such error detectors can be found in practice. An example of the same is described in U.S. Pat. No. 5,418,789") [column 5 lines 12-19];

- "wherein the steps of generating a serialization clock, adding one or more known and controlled amount of jitter to the serialization clock, transmitting a known sequence of test signals using the serialization clock with the added jitter, and causing a clock and data recovery mechanism in the receiver to recover the test signals with jitter are all performed inside the serial transceiver chip" [Fig 2 illustrates several components whose operations are performed inside of a serial transceiver chip].

- "adding one or more known and controlled amount of jitter is performed by use of an interpolator and an interpolator control mechanism programmed to create the known and controlled amount of jitter" (i.e. "It is preferred that the data generator generates an arbitrary (pseudo random) data stream. In the present invention the timing of the clock is jittered by frequency or phase modulation") [column 4 lines 20-23].

Claim 8:

Dalmia et al. disclose a method of testing a serial transceiver chip for jitter tolerance, the transceiver including at least one transmitter and at least one receiver, as in Claim 5 above, further comprising,

- "the known sequence of test signals is created inside the serial transceiver chip" (i.e. "The jitter test determines whether the CRU can correctly recover the data from the data stream that is generated from the specifically jittered clock") [column 3 lines 32-34];

- "comparing the recovered sequence of test signals is also performed inside the serial transceiver chip" (i.e. "The error detection circuit 3 checks the recovered data stream for bit errors, the output thereof being an indication of the bits in error. Several realizations of such error detectors can be found in practice. An example of the same is described in U.S. Pat. No. 5,418,789") [column 5 lines 12-19].

Claim 13:

Dalmia et al. disclose a method of testing a serial receiver for jitter tolerance, the serial receiver being fully contained on a single semiconductor substrate comprising,

- "generating a known sequence of test signals containing negligible jitter relative to a local reference clock" (i.e. "The data generator 2 generates a data stream in a well known manner, the data timing of which is controlled by a clock signal received at the clock input of the data generator") [column 3 lines 17-19];

- "causing a clock and data recovery mechanism in the serial receiver to recover the test signals" (i.e. "The jitter test determines whether the CRU can correctly recover the data from the data stream that is generated from the specifically jittered clock") [column 3 lines 32-34];

- "adding one or more known and controlled amount of jitter into the clock recovery mechanism to force the clock recovery mechanism to compensate for the added jitter" (i.e. "It is preferred that the data generator generates an arbitrary (pseudo random) data stream. In the present invention the timing of the clock is jittered by frequency or phase modulation") [column 4 lines 20-23];

- "comparing the recovered test signals with said known sequence of test signals thereby

  testing the ability of the clock and data recovery mechanism to tolerate the jitter that was

  added" (i.e. "The error detection circuit 3 checks the recovered data stream for bit errors,

  the output thereof being an indication of the bits in error. Several realizations of such

  error detectors can be found in practice. An example of the same is described in U.S. Pat.

  No. 5,418,789") [column 5 lines 12-19];

- "wherein the steps of causing a clock and data recovery mechanism in the receiver to

  recover the test signals, and adding the known and controlled amount of jitter to the clock

  recovery mechanism are all performed inside the serial receiver" [Fig 2 illustrates several

  components whose operations are performed inside of a serial transceiver chip].

- "adding one or more known and controlled amount of jitter is performed by use of an

  interpolator control mechanism programmed to create the known and controlled amount

  of jitter" (i.e. "It is preferred that the data generator generates an arbitrary (pseudo

  random) data stream. In the present invention the timing of the clock is jittered by

  frequency or phase modulation") [column 4 lines 20-23].

Claim 16:

Dalmia et al. disclose a method of testing a serial receiver for jitter tolerance, the serial receiver

being fully contained on a single semiconductor substrate, as in Claim 13 above, further

comprising,

- "comparing the recovered sequence of test signals is performed inside the serial receiver"

  (i.e. "The error detection circuit 3 checks the recovered data stream for bit errors, the

output thereof being an indication of the bits in error. Several realizations of such error

detectors can be found in practice. An example of the same is described in U.S. Pat. No.

5,418,789") [column 5 lines 12-19].

Claim 18:

<u>Dalmia et al.</u> disclose a method of testing a serial transceiver for jitter transfer, the serial

transceiver including at least one transmitter and at least one receiver, the serial transceiver being

fully contained on a single semiconductor substrate comprising,

- "generating a serialization clock" (i.e. "The data generator 2 generates a data stream in a
  well known manner, the data timing of which is controlled by a clock signal received at
  the clock input of the data generator") [column 3 lines 17-19];

- "adding one or more known and controlled amounts of jitter to the serialization clock"
  (i.e. "It is preferred that the data generator generates an arbitrary (pseudo random) data
  stream. In the present invention the timing of the clock is jittered by frequency or phase
  modulation") [column 4 lines 20-23];

- "transmitting a sequence of test signals using the serialization clock with the added jitter"
  (i.e. "This provides a jitter of known characteristics of frequency or frequency and
  amplitude on the clock. The result is a jittered clock output, which is applied to the clock
  input of the data generator 2") [column 3 lines 27-31];

- "causing a clock and data recovery mechanism in a receiver to recover a clock signal
  from the transmitted sequence of test signals" (i.e. "The jitter test determines whether the
  CRU can correctly recover the data from the data stream that is generated from the
  specifically jittered clock") [column 3 lines 32-34];

- "monitoring and measuring an amount of jitter present in the recovered clock signal" (i.e. "The test thus is comprised of the steps of generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER TESTER 3 the number of bit errors that arise in the CRU's recovered data stream. The tolerance or lack of tolerance of the CRU to jitter can be thereby established") [column 4 lines 34-40];

- "comparing jitter present in the recovered clock with jitter added to the serialization clock thereby testing the jitter transfer characteristic of the transceiver" (i.e. "The error detection circuit 3 checks the recovered data stream for bit errors, the output thereof being an indication of the bits in error. Several realizations of such error detectors can be found in practice. An example of the same is described in U.S. Pat. No. 5,418,789") [column 5 lines 12-19];

- "wherein the steps of generating a serialization clock, adding jitter to the serialization clock, transmitting a sequence of test signals, monitoring and measuring an amount of jitter in the recovered clock signal, and comparing jitter present in the recovered clock with jitter added to the serialization clock are all performed inside the serial transceiver" [Fig 2 illustrates several components whose operations are performed inside of a serial transceiver chip].

- "adding one or more known and controlled amounts of jitter is performed by use of an interpolator and an interpolator control mechanism programmed to create the known and controlled amounts of jitter" (i.e. "It is preferred that the data generator generates an arbitrary (pseudo random) data stream. In the present invention the timing of the clock is jittered by frequency or phase modulation") [column 4 lines 20-23].

Claim 19:

Dalmia et al. disclose a method of testing a serial transceiver for jitter transfer, the serial transceiver including at least one transmitter and at least one receiver, the serial transceiver being fully contained on a single semiconductor substrate comprising,

- "generating a serialization clock" (i.e. "The data generator 2 generates a data stream in a well known manner, the data timing of which is controlled by a clock signal received at the clock input of the data generator") [column 3 lines 17-19];

- "adding one or more known and controlled amounts of jitter to the serialization clock" (i.e. "It is preferred that the data generator generates an arbitrary (pseudo random) data stream. In the present invention the timing of the clock is jittered by frequency or phase modulation") [column 4 lines 20-23];

- "transmitting a sequence of test signals using the serialization clock with the added jitter" (i.e. "This provides a jitter of known characteristics of frequency or frequency and amplitude on the clock. The result is a jittered clock output, which is applied to the clock input of the data generator 2") [column 3 lines 27-31];

- "causing a clock and data recovery mechanism in a receiver to recover a clock signal from the transmitted sequence of test signals" (i.e. "The jitter test determines whether the CRU can correctly recover the data from the data stream that is generated from the specifically jittered clock") [column 3 lines 32-34];

- "monitoring and measuring an amount of jitter present in the recovered clock signal" (i.e. "The test thus is comprised of the steps of generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER TESTER 3 the number of bit errors that arise in the CRU's recovered data stream. The tolerance or lack of tolerance of the CRU to jitter can be thereby established") [column 4 lines 34-40];

- "comparing jitter present in the recovered clock with jitter added to the serialization clock thereby testing the jitter transfer characteristic of the transceiver" (i.e. "The error detection circuit 3 checks the recovered data stream for bit errors, the output thereof being an indication of the bits in error. Several realizations of such error detectors can be found in practice. An example of the same is described in U.S. Pat. No. 5,418,789") [column 5 lines 12-19];

- "wherein the steps of generating a serialization clock, adding jitter to the serialization clock, transmitting a sequence of test signals, monitoring and measuring an amount of jitter in the recovered clock signal, and comparing jitter present in the recovered clock with jitter added to the serialization clock are all performed inside the serial transceiver" [Fig 2 illustrates several components whose operations are performed inside of a serial transceiver chip].

- "monitoring and measuring the amount of jitter present in the recovered clock signal is

  performed by use of an up/down counter that is responsive to direction and step control

  signals for an interpolator used for clock recovery" (i.e. "The test thus is comprised of the

  steps of generating a jittered clock, using the jittered clock to generate a test data stream,

  feeding the test data stream to the CRU that is under test, and determining by the BER

  TESTER 3 the number of bit errors that arise in the CRU's recovered data stream. The

  tolerance or lack of tolerance of the CRU to jitter can be thereby established") [column 4

  lines 34-40];

- "comparing the jitter present in the recovered clock signal is performed by use of a

  programmable comparator set to issue a warning if a maximum count achieved by an

  up/down counter exceeds the maximum allowed to pass the transfer test" (i.e. "The error

  detection circuit 3 checks the recovered data stream for bit errors, the output thereof

  being an indication of the bits in error. Several realizations of such error detectors can be

  found in practice. An example of the same is described in U.S. Pat. No. 5,418,789")

  [column 5 lines 12-19].

Claim 20:

Dalmia et al. disclose a method of testing a serial transceiver for jitter transfer, the serial

transceiver including at least one transmitter and at least one receiver, the serial transceiver being

fully contained on a single semiconductor substrate comprising,

- "generating a serialization clock" (i.e. "The data generator 2 generates a data stream in a

  well known manner, the data timing of which is controlled by a clock signal received at

  the clock input of the data generator") [column 3 lines 17-19];

- "adding one or more known and controlled amounts of jitter to the serialization clock"
  (i.e. "It is preferred that the data generator generates an arbitrary (pseudo random) data
  stream. In the present invention the timing of the clock is jittered by frequency or phase
  modulation") [column 4 lines 20-23];

- "transmitting a sequence of test signals using the serialization clock with the added jitter"
  (i.e. "This provides a jitter of known characteristics of frequency or frequency and
  amplitude on the clock. The result is a jittered clock output, which is applied to the clock
  input of the data generator 2") [column 3 lines 27-31];

- "causing a clock and data recovery mechanism in a receiver to recover a clock signal
  from the transmitted sequence of test signals" (i.e. "The jitter test determines whether the
  CRU can correctly recover the data from the data stream that is generated from the
  specifically jittered clock") [column 3 lines 32-34];

- "monitoring and measuring an amount of jitter present in the recovered clock signal" (i.e.
  "The test thus is comprised of the steps of generating a jittered clock, using the jittered
  clock to generate a test data stream, feeding the test data stream to the CRU that is under
  test, and determining by the BER TESTER 3 the number of bit errors that arise in the
  CRU's recovered data stream. The tolerance or lack of tolerance of the CRU to jitter can
  be thereby established") [column 4 lines 34-40];

- "comparing jitter present in the recovered clock with jitter added to the serialization clock thereby testing the jitter transfer characteristic of the transceiver" (i.e. "The error detection circuit 3 checks the recovered data stream for bit errors, the output thereof being an indication of the bits in error. Several realizations of such error detectors can be found in practice. An example of the same is described in U.S. Pat. No. 5,418,789") [column 5 lines 12-19];

- "wherein the steps of generating a serialization clock, adding jitter to the serialization clock, transmitting a sequence of test signals, monitoring and measuring an amount of jitter in the recovered clock signal, and comparing jitter present in the recovered clock with jitter added to the serialization clock are all performed inside the serial transceiver" [Fig 2 illustrates several components whose operations are performed inside of a serial transceiver chip].

- "adding one or more known and controlled amounts of jitter is performed by use of an interpolator and an interpolator control mechanism programmed to create the known and controlled amounts of jitter" (i.e. "It is preferred that the data generator generates an arbitrary (pseudo random) data stream. In the present invention the timing of the clock is jittered by frequency or phase modulation") [column 4 lines 20-23];

- "monitoring and measuring the amount of jitter present in the recovered clock signal is performed by use of an up/down counter that is responsive to direction and step control signals for the interpolator used for clock recovery" (i.e. "The test thus is comprised of the steps of generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the

BER TESTER 3 the number of bit errors that arise in the CRU's recovered data stream.

The tolerance or lack of tolerance of the CRU to jitter can be thereby established")

[column 4 lines 34-40];

- "comparing jitter present in the recovered clock with jitter added to the serialization clock

is performed by use of a programmable comparator that is set to issue a warning if a

maximum count achieved by an up/down counter exceeds a maximum allowed to pass a

transfer test" (i.e. "The error detection circuit 3 checks the recovered data stream for bit

errors, the output thereof being an indication of the bits in error. Several realizations of

such error detectors can be found in practice. An example of the same is described in

U.S. Pat. No. 5,418,789") [column 5 lines 12-19].

Claim 21:

Dalmia et al. disclose a method of testing a serial transceiver for jitter transfer, the serial

transceiver including at least one transmitter and at least one receiver, the serial transceiver being

fully contained on a single semiconductor substrate, as in Claim 20 above, further comprising,

- "the sequence of test signals are generated on the single semiconductor substrate that also

contains the transceiver" (i.e. "The test thus is comprised of the steps of generating a

jittered clock, using the jittered clock to generate a test data stream, feeding the test data

stream to the CRU that is under test, and determining by the BER TESTER 3 the number

of bit errors that arise in the CRU's recovered data stream") [column 3 lines 34-39].

Claim 24:

Dalmia et al. disclose a method of testing a serial receiver for jitter transfer, the serial receiver

being fully contained on a single semiconductor substrate comprising,

- "generating a sequence of test signals containing negligible jitter relative to a local

  reference clock" (i.e. "The data generator 2 generates a data stream in a well known

  manner, the data timing of which is controlled by a clock signal received at the clock

  input of the data generator") [column 3 lines 17-19];

- "causing a clock recovery mechanism in the serial receiver to recover a clock signal from

  the sequence of test signals" (i.e. "The jitter test determines whether the CRU can

  correctly recover the data from the data stream that is generated from the specifically

  jittered clock") [column 3 lines 32-34];

- "the clock recovery mechanism contained on the single semiconductor substrate" [Fig 2

  illustrates a clock recovery mechanism on a single semiconductor substrate];

- "adding one or more known and controlled amounts of jitter into the clock recovery

  mechanism to force the clock recovery mechanism to compensate for added jitter" (i.e.

  "It is preferred that the data generator generates an arbitrary (pseudo random) data

  stream. In the present invention the timing of the clock is jittered by frequency or phase

  modulation") [column 4 lines 20-23];

- "monitoring and measuring an amount of activity in the clock recovery mechanism" (i.e.

  "The test thus is comprised of the steps of generating a jittered clock, using the jittered

  clock to generate a test data stream, feeding the test data stream to the CRU that is under

test, and determining by the BER TESTER 3 the number of bit errors that arise in the

CRU's recovered data stream. The tolerance or lack of tolerance of the CRU to jitter can

be thereby established") [column 4 lines 34-40];

- "comparing the amount of activity in the clock recovery mechanism with an expected

    amount of activity that is based on the jitter added thereby testing a jitter transfer

    characteristic of the receiver" (i.e. "The error detection circuit 3 checks the recovered

    data stream for bit errors, the output thereof being an indication of the bits in error.

    Several realizations of such error detectors can be found in practice. An example of the

    same is described in U.S. Pat. No. 5,418,789") [column 5 lines 12-19];

- "wherein the steps of adding one or more known and controlled amounts of jitter into the

    clock recovery mechanism, monitoring and measuring an amount of activity in the clock

    recovery mechanism, and comparing the amount of activity in the clock recovery

    mechanism with an expected amount of activity are all performed inside the serial

    receiver" [Fig 2 illustrates several components whose operations are performed inside of

    a serial transceiver chip].

- "adding one or more known and controlled amounts of jitter is performed by use of an

    interpolator control mechanism that is programmed to create the known and controlled

    amounts of jitter" (i.e. "It is preferred that the data generator generates an arbitrary

    (pseudo random) data stream. In the present invention the timing of the clock is jittered

    by frequency or phase modulation") [column 4 lines 20-23].

Claim 25:

Dalmia et al. disclose a method of testing a serial receiver for jitter transfer, the serial receiver

being fully contained on a single semiconductor substrate, as in Claim 24 above, further

comprising,

- "monitoring and measuring the amount of activity in the clock recovery mechanism is

  performed by use of an up/down counter that is responsive to direction and step control

  signals for an interpolator used for clock recovery" (i.e. "The test thus is comprised of the

  steps of generating a jittered clock, using the jittered clock to generate a test data stream,

  feeding the test data stream to the CRU that is under test, and determining by the BER

  TESTER 3 the number of bit errors that arise in the CRU's recovered data stream. The

  tolerance or lack of tolerance of the CRU to jitter can be thereby established") [column 4

  lines 34-40];

- "comparing the amount of activity in the clock recovery mechanism with the expected

  amount of activity is performed by use of a programmable comparator set to issue a

  warning if a maximum count achieved by an up/down counter exceeds the maximum

  allowed to pass the transfer test" (i.e. "The error detection circuit 3 checks the recovered

  data stream for bit errors, the output thereof being an indication of the bits in error.

  Several realizations of such error detectors can be found in practice. An example of the

  same is described in U.S. Pat. No. 5,418,789") [column 5 lines 12-19].

Claim 26:

Dalmia et al. disclose a method of testing a serial receiver for jitter transfer, the serial receiver

being fully contained on a single semiconductor substrate comprising,

-   "generating a sequence of test signals containing negligible jitter relative to a local

    reference clock" (i.e. "The data generator 2 generates a data stream in a well known

    manner, the data timing of which is controlled by a clock signal received at the clock

    input of the data generator") [column 3 lines 17-19];

-   "causing a clock recovery mechanism in the serial receiver to recover a clock signal from

    the sequence of test signals" (i.e. "The jitter test determines whether the CRU can

    correctly recover the data from the data stream that is generated from the specifically

    jittered clock") [column 3 lines 32-34];

-   "the clock recovery mechanism contained on the single semiconductor substrate" [Fig 2

    illustrates a clock recovery mechanism on a single semiconductor substrate];

-   "adding one or more known and controlled amounts of jitter into the clock recovery

    mechanism to force the clock recovery mechanism to compensate for added jitter" (i.e.

    "It is preferred that the data generator generates an arbitrary (pseudo random) data

    stream. In the present invention the timing of the clock is jittered by frequency or phase

    modulation") [column 4 lines 20-23];

-   "monitoring and measuring an amount of activity in the clock recovery mechanism" (i.e.

    "The test thus is comprised of the steps of generating a jittered clock, using the jittered

    clock to generate a test data stream, feeding the test data stream to the CRU that is under

test, and determining by the BER TESTER 3 the number of bit errors that arise in the

CRU's recovered data stream. The tolerance or lack of tolerance of the CRU to jitter can

be thereby established") [column 4 lines 34-40];

- "comparing the amount of activity in the clock recovery mechanism with an expected

  amount of activity that is based on the jitter added thereby testing a jitter transfer

  characteristic of the receiver" (i.e. "The error detection circuit 3 checks the recovered

  data stream for bit errors, the output thereof being an indication of the bits in error.

  Several realizations of such error detectors can be found in practice. An example of the

  same is described in U.S. Pat. No. 5,418,789") [column 5 lines 12-19];

- "wherein the steps of adding one or more known and controlled amounts of jitter into the

  clock recovery mechanism, monitoring and measuring an amount of activity in the clock

  recovery mechanism, and comparing the amount of activity in the clock recovery

  mechanism with an expected amount of activity are all performed inside the serial

  receiver" [Fig 2 illustrates several components whose operations are performed inside of

  a serial transceiver chip].

- "monitoring and measuring the amount of activity in the clock recovery mechanism is

  performed by use of an up/down counter that is responsive to direction and step control

  signals for an interpolator used for clock recovery" (i.e. "The test thus is comprised of the

  steps of generating a jittered clock, using the jittered clock to generate a test data stream,

  feeding the test data stream to the CRU that is under test, and determining by the BER

TESTER 3 the number of bit errors that arise in the CRU's recovered data stream. The

tolerance or lack of tolerance of the CRU to jitter can be thereby established") [column 4

lines 34-40];

-   "comparing the amount of activity in the clock recovery mechanism with the expected

amount of activity is performed by use of a programmable comparator set to issue a

warning if a maximum count achieved by an up/down counter exceeds the maximum

allowed to pass the transfer test" (i.e. "The error detection circuit 3 checks the recovered

data stream for bit errors, the output thereof being an indication of the bits in error.

Several realizations of such error detectors can be found in practice. An example of the

same is described in U.S. Pat. No. 5,418,789") [column 5 lines 12-19].

Claim 27:

Dalmia et al. disclose a method of testing a serial receiver for jitter transfer, the serial receiver

being fully contained on a single semiconductor substrate, as in Claim 26 above, further

comprising,

-   "the sequence of test signals are generated on the single semiconductor substrate that also

contains the receiver" (i.e. "The test thus is comprised of the steps of generating a jittered

clock, using the jittered clock to generate a test data stream, feeding the test data stream

to the CRU that is under test, and determining by the BER TESTER 3 the number of bit

errors that arise in the CRU's recovered data stream") [column 3 lines 34-39].

Claim 32:

Dalmia et al. disclose a method of testing a FIFO (First In First Out) circuit on a single

semiconductor substrate comprising,

-   "generating an on-chip clock at the same frequency as a reference clock" (i.e. "The data

    generator 2 generates a data stream in a well known manner, the data timing of which is

    controlled by a clock signal received at the clock input of the data generator") [column 3

    lines 17-19];

-   "incrementally adding a known and controlled amount of phase shifts to the on-chip

    clock signal" (i.e. "It is preferred that the data generator generates an arbitrary (pseudo

    random) data stream. In the present invention the timing of the clock is jittered by

    frequency or phase modulation") [column 4 lines 20-23];

-   "using the reference clock and the phase-shifted on-chip clock to drive the FIFO circuit"

    [Fig 3 illustrates a reference clock and a phase-shifted on-chip clock which drives a FIFO

    circuit];

-   "measuring an amount of phase-shift that can be added to the on-chip clock signal before

    the FIFO experiences overflow and/or underflow errors" (i.e. "The test thus is comprised

    of the steps of generating a jittered clock, using the jittered clock to generate a test data

    stream, feeding the test data stream to the CRU that is under test, and determining by the

    BER TESTER 3 the number of bit errors that arise in the CRU's recovered data stream.

    The tolerance or lack of tolerance of the CRU to jitter can be thereby established")

    [column 4 lines 34-40];

- "wherein the steps of generating an on-chip clock, incrementally adding a known and

    controlled amount of phase shifts, using the reference clock and the phase-shifted on-chip

    clock to drive the FIFO circuit, and measuring an amount of phase-shift are all performed

    on the single semiconductor substrate" [Fig 2 illustrates several components whose

    operations are performed inside of a serial transceiver chip].

- "incrementally adding a known and controlled amount of phase shifts is performed by

    use of an interpolator and an interpolator control mechanism programmed to create

    desired phase shifts" (i.e. "It is preferred that the data generator generates an arbitrary

    (pseudo random) data stream. In the present invention the timing of the clock is jittered

    by frequency or phase modulation") [column 4 lines 20-23].

Claim 43:

Dalmia et al. disclose an apparatus for inserting known and controlled amount of jitter onto a

switching signal comprising,

- "an interpolator for inserting the jitter" [Fig 2 illustrates a component for inserting jitter];

- "an interpolator control mechanism programmed to create the desired jitter" (i.e. "It is

    preferred that the data generator generates an arbitrary (pseudo random) data stream. In

    the present invention the timing of the clock is jittered by frequency or phase

    modulation") [column 4 lines 20-23];

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

5.   Claims 6, 7, 14, 15, 33, & 34 rejected under 35 U.S.C. 103(a) as being unpatentable over

Dalmia et al. (US-5835501-A) in view of Fan et al. (US-7093172-B2).

Claim 6:

Dalmia et al. disclose a method of testing a serial transceiver chip for jitter tolerance, the

transceiver including at least one transmitter and at least one receiver, as in Claim 5 above, but

do not disclose,

-   "the known sequence of test signals is created by a PRBS (Pseudo Random Binary

    Sequence) generation mechanism," although Fan et al. do suggest PRBS, as recited

    below;

-   "comparing the recovered test signals is done by use of the PRBS verification

    mechanism," although Fan et al. do suggest PRBS, as recited below;

however, Fan et al. do disclose,

-   "A digital core 225 may also include a pseudo-random bit sequence (PRBS) generator

    225a, a PRBS checker 225b and a window counter 225c. The PRBS checker 225b and

    the window counter 225c may be embodied in a single unit 226 within digital core 225

    although the invention is not limited in this regard" [column 9 lines 29-34];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "the known sequence of test signals is created by a PRBS

(Pseudo Random Binary Sequence) generation mechanism" and "comparing the recovered test

signals is done by use of the PRBS verification mechanism," in the invention as disclosed by

Dalmia et al. since Dalmia et al. suggests the usage of PRBS, "It is preferred that the data

generator generates an arbitrary (pseudo random) data stream" [column 3 lines 20-21].

Claim 7:

Dalmia et al. and Fan et al. disclose a method of testing a serial transceiver chip for jitter

tolerance, the transceiver including at least one transmitter and at least one receiver, as in Claim

6 above, further comprising,

-       "creating the known sequence of test signals and comparing the recovered sequence of

        test signals is performed inside the serial transceiver chip" (i.e. "The jitter test determines

        whether the CRU can correctly recover the data from the data stream that is generated

        from the specifically jittered clock… The error detection circuit 3 checks the recovered

        data stream for bit errors, the output thereof being an indication of the bits in error.

        Several realizations of such error detectors can be found in practice. An example of the

        same is described in U.S. Pat. No. 5,418,789") [column 3 lines 32-34 & column 5 lines

        12-19].

Claim 14:

Dalmia et al. disclose a method of testing a serial receiver for jitter tolerance, the serial receiver being fully contained on a single semiconductor substrate, as in Claim 13 above, but do not disclose,

- "the known sequence of test signals is created by a PRBS (Pseudo Random Binary Sequence) generation mechanism," although Fan et al. do suggest PRBS, as recited below;

- "comparing the recovered test signals is done by use of a PRBS verification mechanism," although Fan et al. do suggest PRBS, as recited below;

however, Fan et al. do disclose,

- "A digital core 225 may also include a pseudo-random bit sequence (PRBS) generator 225a, a PRBS checker 225b and a window counter 225c. The PRBS checker 225b and the window counter 225c may be embodied in a single unit 226 within digital core 225 although the invention is not limited in this regard" [column 9 lines 29-34];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the known sequence of test signals is created by a PRBS (Pseudo Random Binary Sequence) generation mechanism" and "comparing the recovered test signals is done by use of a PRBS verification mechanism," in the invention as disclosed by Dalmia et al. since Dalmia et al. suggests the usage of PRBS, "It is preferred that the data generator generates an arbitrary (pseudo random) data stream" [column 3 lines 20-21].

Claim 15:

Dalmia et al. and Fan et al. disclose a method of testing a serial receiver for jitter tolerance, the serial receiver being fully contained on a single semiconductor substrate, as in Claim 14 above, further comprising,

-   "comparing the recovered sequence of test signals is performed inside the serial receiver" (i.e. "The error detection circuit 3 checks the recovered data stream for bit errors, the output thereof being an indication of the bits in error. Several realizations of such error detectors can be found in practice. An example of the same is described in U.S. Pat. No. 5,418,789") [column 5 lines 12-19].

Claim 33:

Dalmia et al. disclose a method of testing a FIFO (First In First Out) circuit on a single semiconductor substrate, as in Claim 32 above, but do not disclose,

-   "providing a PRBS pattern to be used as input data for the FIFO," although Fan et al. do suggest PRBS, as recited below;

-   "checking output data from the FIFO with a PRBS verifier," although Fan et al. do suggest PRBS, as recited below;

-   "the PRBS verifier being disposed on the single semiconductor substrate," although Fan et al. do suggest PRBS, as recited below;

however, Fan et al. do disclose,

- "A digital core 225 may also include a pseudo-random bit sequence (PRBS) generator
  225a, a PRBS checker 225b and a window counter 225c. The PRBS checker 225b and
  the window counter 225c may be embodied in a single unit 226 within digital core 225
  although the invention is not limited in this regard" [column 9 lines 29-34];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "providing a PRBS pattern to be used as input data for the

FIFO" and "checking output data from the FIFO with a PRBS verifier" and "the PRBS verifier

being disposed on the single semiconductor substrate," in the invention as disclosed by Dalmia et

al. since Dalmia et al. suggests the usage of PRBS, "It is preferred that the data generator

generates an arbitrary (pseudo random) data stream" [column 3 lines 20-21].

Claim 34:

Dalmia et al. and Fan et al. disclose a method of testing a serial receiver for jitter tolerance, the

serial receiver being fully contained on a single semiconductor substrate, as in Claim 33 above,

but Dalmia et al. do not disclose,

- "the PRBS pattern is provided by an on-chip PRBS generator clocked by the reference
  clock signal," although Fan et al. do suggest PRBS, as recited below;

however, Fan et al. do disclose,

- "A digital core 225 may also include a pseudo-random bit sequence (PRBS) generator
  225a, a PRBS checker 225b and a window counter 225c. The PRBS checker 225b and
  the window counter 225c may be embodied in a single unit 226 within digital core 225
  although the invention is not limited in this regard" [column 9 lines 29-34];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "the PRBS pattern is provided by an on-chip PRBS generator

clocked by the reference clock signal," in the invention as disclosed by Dalmia et al. since

Dalmia et al. suggests the usage of PRBS, "It is preferred that the data generator generates an

arbitrary (pseudo random) data stream" [column 3 lines 20-21].

Response to Arguments

6.   Applicant's arguments filed 01/15/2007 have been fully considered but they are not

persuasive.

        In response to applicant's argument that the references fail to show certain features of

applicant's invention, it is noted that the features upon which applicant relies (i.e., "Initially, note

that the exemplary interpolator set forth in the Specification, shown in Figures 3A and 3B, is a

digital circuit that receives four phase signals, P_0, P_{90}, P_{180}, and P_{270}, and under control of control

signals SCO, SC1 , TCO and TC1 selects and combines the phase signals in a manner that allows

insertion of the desired frequency and magnitude components of jitter onto the transmit clock.

Thus, the recited interpolator not only eliminates the requirement for analog circuitry for jitter

generation, but also allows such jitter to be generated with digital precision that allows for jitter

transfer measurement by a receiver that includes a counterpart interpolator (see, e.g.,

Specification, paragraphs [0089]-[0099]). By contrast, Dalmia et al. disclose a prior art analog

jitter generator wherein a sine wave modulates a VCO. They disclose no awareness of an

interpolator nor the benefits of using an interpolator in jitter generation") are not recited in the

rejected claim(s) (i.e. "adding one or more known and controlled amount of jitter is performed

by use of an interpolator and an interpolator control mechanism programmed to create the known

and controlled amount of jitter"). Although the claims are interpreted in light of the

specification, limitations from the specification are not read into the claims. See *In re Van

Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The examiner notes that the applicant's arguments recite more explicit limitations than

those recited in the current claim language.   The current claim language is interpreted by the

examiner as providing coverage for controlling an amount of desired jitter by signal

interpolation.

Conclusion

7.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing

date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Oscar Louie whose telephone number is 571-270-1684. The examiner can normally be reached Monday through Thursday from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami, can be reached at 571-272-4195. The fax phone number for Formal or Official faxes to Technology Center 2100 is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

OAL
03/21/2008

/Nasser G Moazzami/
Supervisory Patent Examiner, Art Unit 2136